



For Immediate Release:

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**Austin Semiconductor, Inc. launches new iPEM Product family member
2.4Gb, SDRAM-DDR in 219-PBGA**

Austin, Texas - Austin Semiconductor, Inc. (ASI), a leading supplier of high reliability (HI-REL) as well as, ruggedized plastic encapsulated semiconductor products and services, announces the release of its second synchronous DRAM, double data-rate member of its iPEM product family and the upgrade to the 1.2Gb, 16M x 72, SDRAM-DDR PBGA released in June of this year. This Austin Semiconductor product family is based on integrated multiple silicon devices, manufactured on an organic laminate micro-substrate and then encapsulated using industry standard plastic materials (iPEM).

This Austin Semiconductor product introduction is a multi-chip (die) SDRAM-DDR with a total density of 2.4Gb and organized as 32M x 72/80, fitting a footprint of 32mm x 25mm and containing a total of 219 balls which constitutes the electro-mechanical interface.

This product is available today, currently sampling DDR266 devices at full military temperature range and DDR333 devices available for the industrial temperature range, production orders are being accepted now, lead-time and unit pricing available via all Austin Semiconductor sales channels. A complete datasheet is available for download at www.austinsemiconductor.com. ASI continues to show their support to HI-REL markets by continuously developing products defined for use in these environments, such as the AS4DDR16M72PBG. The iPEM product family will greatly increase the number plastic encapsulated products offered and enhance Austin's already comprehensive product and services offering

AS4DDR32M72PBG features include:

- Total Density: 2.4Gb Organized as 32M x 72/80
- DDR SDRAM, Data Rate = 200, 250, 266 and 333 Mbps (Million Bits per Second)
- Core Frequencies = 100, 125, 133 and 166 MHz
- 2.5V +/- 0.2V Power Supply
- 2.5V I/O Supply (SSTL_2 compatible)
- Differential Input Clocks (CLK and CLK\)
- Internal Pipelined, DDR Architecture; Two Data Accesses Per Clock Cycle
- Commands Entered on the Rising Clock Edge (CLK)
- Programmable Burst Length = 2, 4 or 8
- Bi-Directional Data Strobe (DQS)
- DQS Edge-Aligned with Data for READ; Center Aligned with Data for WRITE
- DLL to Align DQ and DQS Transitions with Input Clocks
- Multi-Bank Internal Architecture Supporting Concurrent Operation
- Data Mask Inputs Per Byte (DQMLx and DQMHx)
- Programmable Output Drive (IOH/IOL)
- Auto Precharge, Auto Refresh and Self Refresh (Industrial only)

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Austin Semiconductor, Inc. (ASI) is progressively changing the component availability landscape for integrated components for use in Hi-Reliability and harsh environments. We have an aggressive development plan to introduce multiple SDRAM, SRAM and Mixed memory iPEM definitions over the next year and in addition are currently in-process of defining System in Package offerings (SiP). For more information on our iPEM product offerings, please contact us or visit our newly enhanced website.

Austin Semiconductor, Inc. (ASI) is a fully QML certified, ISO registered company that supports the high reliability requirements of industries including Military, Aerospace, Transportation and Medical¹. ASI offers I/C components and modules / MCM's to their customers through a broad line of HI-REL and COTS products composed of standard & specialty memory and digital & analog solutions that are available in a wide array of ceramic and plastic packages. ASI also offers DMS services, obsolescence support and radiation tolerant products. ASI designs, develops and manufactures these products exclusively for the global HI-REL marketplace and service industry.

For additional information, contact:
David Harrison, VP of Market Development
dharrison@austinsemiconductor.com
Main: 512.339.1188 x7169
Direct: 603.472.7477
Mobile:508.380.0495

¹ Diagnostic/Monitoring, Non-Life support Medical Applications

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